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EXAMINER	
LINDLOF, JOHN M	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/601,172	ROHLMAN ET AL.	
	Examiner	Art Unit	
	JOHN LINDLOF	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *30* is/are allowed.

6)☒ Claim(s) *28,29 and 31-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 28-42 are presented for examination.

Response to Arguments

Applicant's arguments, see Argument after Notice of Appeal, filed 2/2/2009, with respect to the rejection(s) of claims 28, 29, and 31-42 under 35 U.S.C. 103(a) have been fully considered and are persuasive due to both the Gottlieb reference and the present application being assigned, or subject to an obligation of assignment, to Intel Corporation at the time the present invention was made. Therefore, the final rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Borkenhagen (U.S. Patent No. 6,088,788) in view of Agarwal et al., "Sparcle: An Evolutionary Processor Design for Large-Scale Multiprocessors" (hereinafter Agarwal), further in view of Hervin (U.S. Patent No. 6,138,230).

2. As per claim 28, Borkenhagen discloses an instruction pipeline in a microprocessor, comprising: a plurality of pipeline units, each of the pipeline units configured to process instructions (col 8 lines 33-52), wherein: the instructions are distributed in multiple threads for the plurality of pipeline units to process (col 4 lines 9-32 and fig. 5);

And at least one of the plurality of pipeline units is configured to:

Receive an instruction from another of the pipeline units;

Issue the received instruction to a downstream pipeline unit (fig. 7; fig 10A);

Borkenhagen fails to disclose details regarding the instructions that are in the pipeline when a thread is switched and that a copy of the instruction is stored in response to the receipt of the instruction.

Agarwal discloses the requirement for instructions currently in the pipeline to be flushed as well as saving the architectural state of the processor during a switch (see e.g. pg. 11).

Likely the processing system of Borkenhagen was intended to utilize this technique. Flushing instructions that are fetched, but not yet committed, when a thread switch occurs is overwhelmingly typical. The requirement of a flushed instruction does not appear to be inherent. None of the references used in the rejection utilize a technique that prevents these instructions from being flushed, but Examiner does not deny this possibility that such an invention exists. For that reason, the rejection is an obvious rejection in view of Agarwal rather than an anticipatory rejection. Borkenhagen

would have been motivated to allow these particular instructions to be flushed to ensure proper execution of instructions. Similarly, Borkenhagen would be motivated to save the context of the thread to improve efficiency within the processing system.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Borkenhagen and utilize the flushing technique and context saving of Agarwal.

Borkenhagen/Agarwal fails to explicitly disclose saving a copy of the instruction in response to receiving an instruction (rather than being potentially responsive to a thread switch).

Hervin discloses a method of saving the context of an instruction by checkpointing (col 19 lines 28-49)

Borkenhagen/Agarwal would have been motivated to utilize this technique for context saving because it will allow for faster thread switches. Instead of waiting for a known thread switch to save a context, checkpointing may be done on response to receiving the instruction so it is ready when a cache miss occurs.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Borkenhagen/Agarwal and allow saving a copy of instructions within the pipeline in response to receiving an instruction. This may occur with particular instructions or with every instruction (Hervin col 19 lines 42-44).

3. Claims 29, 31-36 and 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkenhagen/Agarwal/Hervin in view of Flynn et al. (U.S. Patent No. 5,907,702) hereinafter referred to as Flynn.

4. As per claim 29, Borkenhagen/Agarwal/Hervin discloses an instruction pipeline in a microprocessor, comprising:

at least one upstream pipeline unit (fetch/dispatch stage Col. 1 lines 50-62) configured to issue each of a series of instructions on one of a plurality of instruction threads; (Col. 3 line 13 – col. 4 line 39)

at least one downstream pipeline unit (stages 1-3 of fig. 5 and Col. 1 line 63- col. 2 line 8) configured to allocate each of the series of instructions on the one of the plurality of instruction threads on which each of the series of instructions were issued; *The examiner asserts that each instruction is allocated registers depending on the thread on which it was issued (Col. 3 lines 18-42).*

reissuing to the at least one downstream pipeline unit at least one of the series of instructions on the one of the plurality of instruction threads on which the at least one of the series of instructions was issued. (Col. 4 lines 4-39)

5. Borkenhagen/Agarwal/Hervin fails to disclose an instruction queue, wherein in a first operating mode, the instruction queue being configured to pass each of the series of instruction from the at least one upstream pipeline unit to the at least one downstream pipeline unit on the one of the plurality of instruction threads on which each of the series of instructions were issued and configured to store each of the series of

instructions, at least one memory location being dedicated to each of the plurality of instruction threads.

6. Flynn discloses an instruction queue (Fig. 2 queues 10 and 14), wherein in a first operating mode, the instruction queue being configured to pass each of the series of instruction from the at least one upstream pipeline unit to the at least one downstream pipeline unit on the one of the plurality of instruction threads on which each of the series of instructions were issued and configured to store each of the series of instructions, at least one memory location being dedicated to each of the plurality of instruction threads. (Col. 3 lines 27-38) *The examiner asserts that each instruction stored in the queue inherently occupies a memory location defined by the size of the instruction.*

7. Flynn teaches that his invention "decreases thread switching latency in a multithreaded processor" (Col. 1 lines 9-10) which is a desired outcome of Borkenhagen/Agarwal/Hervin's invention (Borkenhagen col. 1 lines 30-32).

8. It would have been obvious to one of ordinary skill in the art at the time of invention to have replaced Borkenhagen/Agarwal/Hervin's fetch and dispatch stages with Flynn's fetch and dispatch method and apparatus for the benefit of decreased thread switching latency.

9. As per claim 31, Borkenhagen/Agarwal/Hervin/Flynn disclose the instruction pipeline of claim 29, wherein the at least one upstream pipeline unit is configured to determine the one of the plurality of instruction threads on which to issue each of the series of instructions based the availability of resources on each of the plurality of

instruction threads. *The examiner asserts that a series of instructions is assigned to a specific thread based on that thread not already processing a second series of instructions.*

10. As per claim 32, Borkenhagen/Agarwal/Hervin discloses method of processing instructions in a multi-threaded instruction pipeline, comprising: issuing, from an upstream pipeline unit, instructions on one of a plurality of instruction threads and passing the issued instructions to a downstream unit on the one of the plurality of instruction threads (Col. 1 line 63- col. 2 line 8); detecting a stall in the one of the plurality of instruction threads; and after detecting the stall, reissuing at least one of the issued instructions, on the one of the plurality of instruction threads on which the instructions were issued. (Col. 4 lines 4-39)

11. Borkenhagen/Agarwal/Hervin fails to disclose storing the issued instructions in a queue.

12. Flynn discloses storing the issued instructions in a queue (Fig. 2 queues 10 and 14) and issuing instructions from said queue. (Col. 3 lines 27-38)

13. Flynn teaches that his invention "decreases thread switching latency in a multithreaded processor" (Col. 1 lines 9-10) which is a desired outcome of Borkenhagen/Agarwal/Hervin's invention (Borkenhagen col. 1 lines 30-32).

14. It would have been obvious to one of ordinary skill in the art at the time of invention to have replaced Borkenhagen/Agarwal/Hervin's fetch and dispatch stages

with Flynn's fetch and dispatch method and apparatus for the benefit of decreased thread switching latency.

15. As per claim 33, Borkenhagen/Agarwal/Hervin/Flynn disclose the method according to claim 32, further comprising: maintaining a respective pointer for each of the plurality of instruction threads, *The examiner asserts that Flynn's invention inherently maintains a pointer to each instruction thread. If it did not, the processor would be unable to fetch instructions from each thread.*

wherein the reissuing step includes reissuing the at least one of the issued instruction from the queue using the respective pointer for the one of the plurality of instruction threads on which the instruction was issued. (Borkenhagen Col. 4 lines 4-39) *The examiner asserts that upon switching back to a first thread from a second, the instruction must be re-fetched before being re-issued. The fetch circuitry will inherently use the thread pointer to fetch from the proper memory location.*

16. As per claim 34, Borkenhagen/Agarwal/Hervin/Flynn disclose the method according to claim 32, further comprising: alternating the issuance of instructions between each of the plurality of instruction threads. *The examiner asserts that the processor alternates between active and dormant threads upon thread switching events (Flynn col. 1 lines 49-51) and that instructions are issued on their proper thread, therefore instruction issuing is also alternated.*

17. As per claim 35, Borkenhagen/Agarwal/Hervin/Flynn disclose the method according to claim 32, further comprising: selecting one of the plurality of instruction threads on which to issue the instructions based on an availability of resources. *The examiner asserts that a series of instructions is assigned to a specific thread based on that thread not already processing a second series of instructions.*

18. As per claim 36, Borkenhagen/Agarwal/Hervin discloses a microprocessor, comprising: a multi-threaded instruction pipeline including at least one upstream pipeline unit configured to issue instructions on a selected one of a plurality of threads of the pipeline (Col. 1 line 63- col. 2 line 8) and to reissue, on the selected one of the plurality of threads, at least one instruction in an event of a downstream stall on the selected one of the plurality of threads. (Col. 4 lines 4-39)

19. Borkenhagen/Agarwal/Hervin fails to disclose an instruction queue configured to pass issued instructions to a downstream pipeline unit on the selected one of the plurality of threads and store a copy of the issued instructions (Hervin col 19 lines 28-49)

20. Flynn discloses an instruction queue (Fig. 2 queues 10 and 14) configured to pass issued instructions to a downstream pipeline unit on the selected one of the plurality of threads and store a copy of the issued instructions (Col. 3 lines 27-38)

21. Flynn teaches that his invention “decreases thread switching latency in a multithreaded processor” (Col. 1 lines 9-10) which is a desired outcome of Borkenhagen/Agarwal/Hervin’s invention (Borkenhagen col. 1 lines 30-32).

22. It would have been obvious to one of ordinary skill in the art at the time of invention to have replaced Borkenhagen/Agarwal/Hervin's fetch and dispatch stages with Flynn's fetch and dispatch method and apparatus for the benefit of decreased thread switching latency.

23. As per claim 38, Borkenhagen/Agarwal/Hervin/Flynn disclose the microprocessor according to claim 36, wherein the downstream pipeline unit includes an execution unit. (Borkenhagen col. 2 lines 2-5)

24. As per claim 39, Borkenhagen/Agarwal/Hervin/Flynn disclose the microprocessor according to claim 36, wherein the instruction queue is configured to select one of the threads based on available resources. *The examiner asserts that a thread is selected for issuance from the queues based on whether the active thread has been stalled or not, which constitutes the availability of downstream resources (pipeline stages) to take a new instruction.*

25. As per claim 40, Borkenhagen/Agarwal/Hervin/Flynn disclose the microprocessor according to claim 36, wherein the instruction queue is configured to alternate between the plurality of threads when passing the instructions. *The examiner asserts that the processor alternates between active and dormant threads upon thread switching events (Flynn col. 1 lines 49-51) and that instructions are issued on their proper thread, therefore instruction issuing is also alternated.*

26. As per claim 41, Borkenhagen/Agarwal/Hervin/Flynn disclose the microprocessor according to claim 36, wherein the instruction queue is configured to pass instructions on one of the threads, and configured to switch to a different one of the threads when a stall is detected on the one of the threads. (Flynn col. 3 lines 28-38)

27. As per claim 42, Borkenhagen/Agarwal/Hervin/Flynn disclose the microprocessor according to claim 36, wherein the instruction queue includes:

a memory device to store the instructions; (Flynn Fig. 2 queues 10 and 14)

and an output multiplexer (Flynn fig. 2 multiplexer 16) which is configured, in a first mode of operation, to pass instructions from the upstream pipeline unit to the downstream pipeline unit, and which is configured, in a second mode of operation, to reissue the at least one of the stored instructions. *The examiner asserts that the multiplexer passes instructions to the subsequent processing stages whether it is their first time being issued or if they being reissued after a stall.*

28. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Borkenhagen/Agarwal/Hervin and Flynn in view of Peleg et al. (U.S. Patent No. 5,381,533) hereinafter referred to as Peleg.

29. As per claim 37, Borkenhagen/Agarwal/Hervin/Flynn disclose the microprocessor according to claim 36, but fail to disclose wherein the at least one upstream pipeline unit includes at least one of a trace cache and a micro-instruction sequencer.

30. Peleg discloses a trace cache (abstract).

31. Peleg teaches that "a plurality of instructions… may be fetched from the cache memory with only one address/access" using a trace cache. (Col. 1 lines 58-61) By using only a single access, the necessity of repeated fetching is eliminated, thereby reducing fetch time, and overall, processing time of an instruction stream.

32. It would have been obvious to one of ordinary skill in the art at the time of invention to have included Peleg's trace cache alongside the instruction cache of Borkenhagen/Agarwal/Hervin/Flynn's processor for the benefit of reduced processing time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN LINDLOF whose telephone number is (571)270-1024. The examiner can normally be reached on Monday-Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

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